DIGITAL BUS MONITOR INTEGRATED CIRCUITS

ABSTRACT OF THE INVENTION

A digital bus monitor used to observe data on a bus (14, 16, 18) connecting multiple integrated circuits (10, 12) comprises a memory buffer (30), bypass register (34), test port (38) and output control circuits (42, 46) controlled by an event qualifying module (EQM) (32). In response to a matching condition the EQM (32) may perform a variety of tests on incoming data while the integrated circuits (10, 12) continue to operate at speed. A plurality of digital bus monitors (20, 22) may be cascaded for observation and test of variable width data buses and variable width signature analysis.